# DIGITAL CONTROL FOR PLLs BASED ON MOVING AVERAGE FILTER: ANALYSIS AND DESIGN IN DISCRETE DOMAIN

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***Abstract* – Phase Locked Loops using phase detector based on a multiplier and a moving average low pass filter are computationally simple, and provide adequate attenuation for the multiplier generated harmonics, which are responsible for distortion at the output signal. They are a good choice for synchronizing power electronics converters connected to the grid. Previously published papers based on proportional-integral control and moving average filter present long settling times. This paper uses the exact model of the moving average filter by its discrete high order transfer function, and applies the discrete root locus method to impose the dominant closed loop poles in a region defined by desired performance specification. It leads to a significantly shorter settling time, when experimentally compared with other recent proposals in the literature.**

***Keywords* - Control Systems, Discrete Time Systems, Phase Locked Loops, Power Electronics, Synchronization.**

## I. INTRODUCTION

Phase Locked Loops (PLLs) are largely employed in grid connected power electronics converters, for instance, renewable energy sources [1], [2]. PLLs based on multiplier type phase detector are usual choices due to their simplicity [3]. However, the multiplier nonlinear behavior produces harmonics which require adequate filtering in order to minimize PLL output distortion. Moving Average (MA) low pass filters are a good choice for software based implementations due to their simplicity and high harmonics attenuation performance.

References [4], [5] present the single and three phase software PLL modeling based on instantaneous vector calculation and orthogonality concept. The MA filter dynamics is approximated to a unity gain, that together with an analogue Proportional-Integral (PI) and the integrator within the Voltage Controlled Oscillator (VCO), results in a second order closed loop system in its canonical form. The PI controller parameters are determined by using the following simple formulas:

$$PI(s) = k_P + \frac{k_I}{s} \tag{1}$$

$$k_P = 2\zeta\omega_c \tag{2}$$

$$k_I = \omega_c^2 \tag{3}$$

where $\omega_c$ is the closed loop crossover frequency and $\zeta$ is the damping factor.

The MA filter approximation presented by [4], [5] is valid for slow PLL transient response design specifications, found in applications such as reference signals generation for a Dynamic Voltage Restorer (DVR) [6], [7]. For applications that require fast PLL transient response (settling time less than three cycles) the controller of [4], [5] does not provide satisfactory results, as the high frequency region of the MA filter transfer function is not adequately modeled with this low order simplified model.

In [8] the PLL controller is designed by inspecting the PLL open loop transfer function Bode diagram, and considering that the damping ratio is determined by:

$$\zeta \approx \frac{PM}{100} \text{ for } PM < 70^o, \tag{4}$$

and the 2% settling time $t_s$ is given by:

$$t_s \approx \frac{4}{\zeta\omega_c}. \tag{5}$$

Reference [8] concludes that, by inspecting the Bode diagram of the PLL open loop transfer function, the PLL transient response can be estimated accurately. However, it is well known that (5) applies only for a second order system and the PLL is a higher order system, thus the method presented in [8] does not estimate the PLL transient response accurately. Moreover, [8] states that MA filters can be used only for slow PLLs, and low controller gains are applied, resulting in poor dynamic performance, as expected.

Reference [9] simplifies the MA filter to a first order low pass filter using Padé approximation, resulting in a third order model for the PLL system. The PI controller is designed based on the symmetric optimum method using the approximated transfer function, assuring stability but without the possibility of imposing time response performance. In spite of using an improved model compared to [4], [5], the high frequency region of the MA filter is still not properly modeled. As a result, transient behavior is not optimized. Previous Authors´ paper [10] presents good transient response by taking into account the MA filter discrete transfer function without discussing the design method. Paper [11] takes the controller design of [10] as a basis and presents a design recipe which allows a fast redesign of the controller for different line and sampling frequencies as well as variation of input voltage $v_i$.

Manuscript received 16/04/2015. First revision 16/07/2015. Accepted for publication 24/09/2015, by recommendation of the Regular Section Editor Cassiano Rech.

The main contribution of this paper is the use of the complete, high order, discrete time domain model of the MA filter without approximations. The closed loop transfer function presents a huge number of poles and zeros, but a pair of dominant complex poles. The design of the PI compensator is based on the placement of this pair of poles to achieve desired value ranges of settling time ( $t_s$ ), damping factor ( $\zeta$ ) and natural frequency ( $\omega_n$ ) for a second order system, by using the discrete root locus method, resulting in significant improvement of the settling time, compared to previous results [4], [5], [8], [9].

The proposed method can be applied for both single and three phase systems [12] and for variable grid frequency operation [13]. The experimental results show good agreement with the expected (analytical) settling times of a second order system.

## II. PLL BASED ON LOW PASS MA-FILTER

Figure 1 presents the discrete time block diagram for the implementation of a single phase PLL whose phase detector consists of a multiplier and a low pass MA filter. The Numerically Controlled Oscillator (NCO) block produces unitary amplitude, sinusoidal signals $v_{o//}$ and $v_o$ with frequency $\omega_o$. The compensator block $F(z)$ assures that $v_{o//}$ will be kept in phase with the input signal $v_i$ and that $v_o$ will be 90° displaced from $v_i$. If the distorted input signal $v_i$ has a fundamental component of amplitude $A_1$ and contains only odd harmonics, the signal $v_{mult}$ can be decomposed into $(A_1/2)\sin(\phi_d)$ and a zero mean term $n(t)$ containing a sum of even harmonics [11], [13] ($\phi_d$ is the phase displacement between $v_i$ and $v_{o//}$). The component $n(t)$ must be sufficiently attenuated by a low pass filter to avoid excessive ripple in $\omega_o$, which would cause undesired odd harmonics in the output signal $v_{o//}$. A $N^{th}$ order MA filter with sampling period $T_s$ calculates the mean value of the last $N$ values of $v_{mult}$ according to:

$$v_f(k) = \frac{1}{N}\sum_{j=1}^{N} v_{mult}(k-j+1). \tag{6}$$

The MA filter transfer function is given by:

$$MA(z) = \frac{v_f(z)}{v_{mult}(z)} = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}. \tag{7}$$

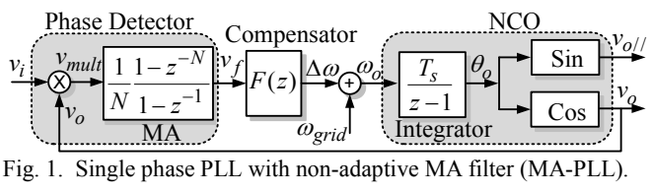

Fig. 1. Single phase PLL with non-adaptive MA filter (MA-PLL).

The MA filter attenuates harmonic components at the multiples of the notch frequency:

$$f_n = (NT_s)^{-1}. \tag{8}$$

If $v_i$ contains only odd harmonics, then $v_{mult}$ has even harmonics, requiring $f_n=2f_1$ [10], where $f_1$ is the fundamental frequency of $v_i$. If $v_i$ contains even and odd harmonics, then $f_n=f_1$. Figure 2 presents the Synchronous Reference Frame three phase PLL (SRF-PLL) where the phase detector multipliers are within the abc/dq block [12]. SRF-PLL tracks the fundamental positive sequence of the input voltages.

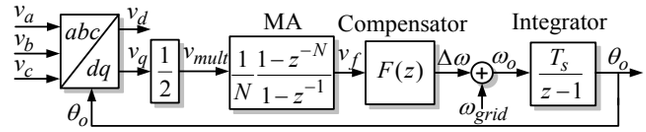

Fig. 2. Three phase PLL with non-adaptive MA filter (MA-PLL).

Figure 3 shows the linearized model of single and three phase PLLs of Figures 1 and 2 [11], [12]. For a three phase PLL, $A_1$ is the amplitude of the positive sequence of the fundamental components of input phase voltages [$v_a$, $v_b$, $v_c$].

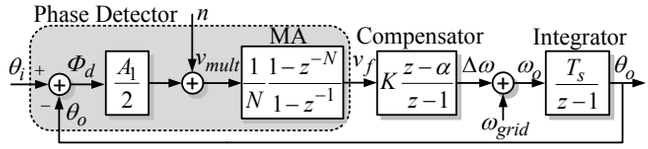

Fig. 3. Linearized discrete model of single and three phase PLLs (MA-PLL).

## III. CONTROLLER DESIGN

The controller design proposed herein is a trial and error strategy based on the z-domain root locus method. The resulting tuned MA filter based PLL has faster transient response when compared with previous methods [4], [5], [8], [9].

Initially, approximate design specifications (damping ratio $\zeta$, natural frequency $\omega_n$ and 2% settling time $t_s$) based on the continuous time second order system, are used as guidelines to place the dominant closed loop poles. According to [14], the specifications above can be translated into the discrete root locus diagram as:

- the closed loop poles for a settling time values lower than $t_s$ should be inside the circle with radius given by:

$$r = e^{-3.91T/t_s} \tag{9}$$

as shown in Figure 4;

- for constant damping ratio $\zeta$, the discrete closed loops should lie on the logarithmic spiral shown in Figure 4;
- for constant natural frequency $\omega_n$, the discrete closed loops should lie on the curve shown in Figure 4.

To satisfy the three specifications above, the closed loop poles should lie on the intersection of the constant damping ratio $\zeta$ and constant natural frequency $\omega_n$ curves shown in Figure 4.

Since the discrete MA filter based PLL is not a second order system, these specifications are not accurate, and can only be used as approximated guidelines to help in the design

procedure, and numerical simulation should be made to verify the system response. Thus, the following parameter variation ranges are defined:

$$\omega_{n1} \le \omega_n \le \omega_{n2} \tag{10}$$

$$\zeta_1 \le \zeta \le \zeta_2 \tag{11}$$

$$t_s \le t_{s1}\,. \tag{12}$$

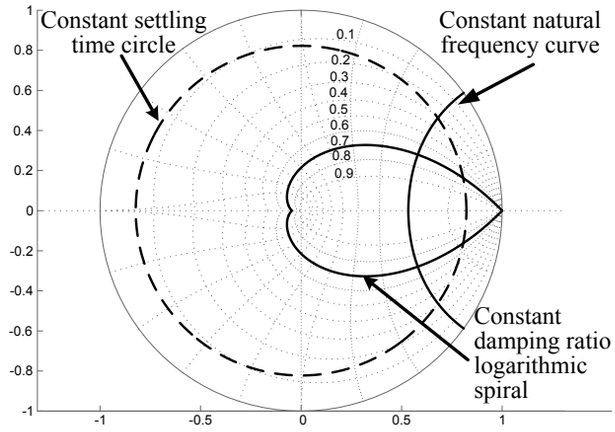


Fig. 4. Root loci for constant $t_s$, $\zeta$ and $\omega_n$.

The parameters $\omega_{n1}$, $\omega_{n2}$, $\zeta_1$, $\zeta_2$, $t_{s1}$ are design specifications that define the permitted regions (shaded regions in Figure 5). The dominant pair of closed loop poles should be placed inside these shaded regions.

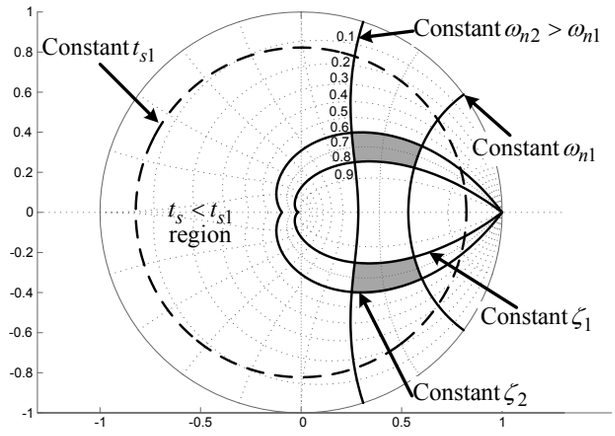


Fig. 5. Permitted regions defined by the root loci of constant $\omega_{n1}$, $\omega_{n2}$, $\zeta_1$, $\zeta_2$, $t_{s1}$ in the Z-domain map.

The applied digital PI controller is:

$$F(z) = k_P + \frac{k_I}{1 - z^{-1}}\,. \tag{13}$$

In order to facilitate the use of the root locus method, (13) is modified to present a multiplying factor ($K$) and a zero ($\alpha$):

$$F(z) = K\frac{z - \alpha}{z - 1} \tag{14}$$

where:

$$K = k_P + k_I \tag{15}$$

$$\alpha = \frac{k_P}{k_P + k_I}\,. \tag{16}$$

The zero location ($\alpha$ adjustment) forces the root locus trajectory to go through the desired shaded region, and gain $K$ is chosen to place the closed loop poles inside the desired shaded region. The open loop transfer function of the MA-PLL is given by:

$$\frac{\theta_o}{\Phi_d} = \frac{A_1 K T_s}{2N} \cdot \frac{z^N - 1}{z^{N-1}(z-1)} \cdot \frac{z - \alpha}{z - 1} \cdot \frac{1}{z - 1}\,. \tag{17}$$

From (17), the MA filter adds $N$ zeros equally displaced over the unitary circle (Figure 6), $N$-1 poles at the origin and one pole at $1+j0$. The PI compensator has one real pole at $1+j0$ and one zero at $\alpha$. The NCO has one real pole at $1+j0$. The open loop poles and zeros and the corresponding closed loop root locus are presented in Figure 6 for $N$=100 samples per period.

The discrete time dominant poles, located in the neighborhood of point ($1+j0$), are shown in Figure 7, a magnified version of Figure 6.

The desired region is defined by the parameters $\omega_{n1} = 20\text{Hz}$, $\omega_{n2} = 35\text{Hz}$, $\zeta_1 = 0.4$, $\zeta_2 = 0.8$, $t_s = 3/60\text{s}$.

Several iterations were needed to impose the dominant closed loop poles in the desired shaded region of Figure 7, followed by step response simulation to check the transient behavior. The final PI controller parameters are $\alpha$=0.99565, $K$=313. Figure 7 also shows the presence of the third dominant pole that makes the second order specifications as approximated guidelines, as stated before.

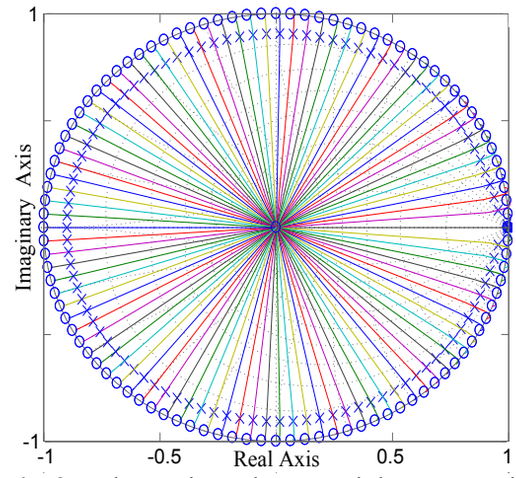


Fig. 6. Open loop poles and zeros and the corresponding closed loop root locus for a MA based PLL.

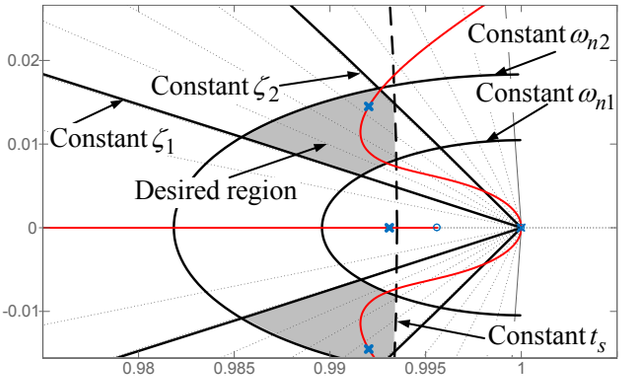


Fig. 7. Detailed view of the Z-domain closed loop root locus for a MA based PLL, around the (1+0*j*) point, showing desired design regions.

## IV. EXPERIMENTAL RESULTS

The proposed PLL controller tuning was experimentally compared with the ones described in [4], [8], [9], for three phase PLLs (Figure 2), using an ARM32F4 floating point processor [13], [15]. Arbitrary real time input test signals were software generated within the processor. Data obtained from processor memory was post processed by using MATLAB to evaluate the phase and frequency settling times and the output phase $\phi_o$. Three tests were performed:

- Test 1 - 0° to 40° phase jump at input $v_i$;
- Test 2 - 60 Hz to 61 Hz frequency jump at input $v_i$;
- Test 3 - 50% voltage sag + 40° phase jump + 10% 5th harmonic+ 10% 7th harmonic at input $v_i$ .

Figure 8 presents experimental waveforms of $v_i$, $v_{o//}$, $\phi_o$ and $\Delta f$, for Tests 1, 2 and 3, for:

- Case 1: the proposed PLL controller tuning;
- Case 2: proposed by [9];
- Case 3: proposed by [8];
- Case 4: proposed by [4].

The variable $\phi_o$ obeys (18):

$$\theta_o = \omega_o t + \phi_o . \tag{18}$$

According to Figure 2, the variable $\Delta f$ is given by (19):

$$\Delta f = \Delta\omega_o / 2\pi = \left(\omega_o - \omega_{grid}\right) / 2\pi = f_o - f_{grid} . \tag{19}$$

Table I summarizes settling times for the three experimental tests.

**TABLE I**
**Comparison of settling time (cycles of nominal frequency) for the three experimental tests.**

| | Case 1 Proposed | Case 2 [9] | Case 3 [8] | Case 4 [4] |
|---|---|---|---|---|
| **Test 1 (phase settling time)** 40° phase jump | 2.08 | 3.73 | 2.22 | 14.01 |
| **Test 2 (frequency settling time)** +1 Hz frequency jump | 2.03 | 3.69 | 2.15 | 13.93 |
| **Test 3 (phase settling time)** 50% sag + 40° phase jump + harmonics | 6.00 | 9.08 | 4.89 | 31.41 |

The settling time definitions are:

- phase settling time for 40° phase jump test is the elapsed time necessary for the phase angle $\phi_o$ to enter and remain in the ±2% band (±0.8°) around 40°;
- frequency settling time for the 1 Hz frequency jump is the elapsed time necessary for the PLL frequency $f_o$ to enter and remain in the ±2% band (±0.02 Hz) around 61 Hz.

The settling times of the proposed PLL and the PLL from [8] for a phase jump at the input signal $v_i$ (Test 1, Cases 1 and 3) are nearly half of the value presented by [9] (Test 1, Case 2).

For the frequency jump test (Test 2), [8] (Case 3) presents a $\Delta f$ settling time comparable to the proposed PLL (Case 1), but its phase error converges to zero only after a very long time more than a hundred cycles (Figure 8, Table I), not visible in Figure 8 time scale.

All the cases in Test 3 present higher phase settling times than Test 1, due to the dependence of the PLL closed loop gain on the amplitude of $v_i$ . Case 3 presents the lower value compared to the others, but presents an extremely high phase settling time for frequency jump.

This confirms that the proposed PLL has the lowest settling for both phase and frequency jump among the tested PLLs.

In order to verify the adequacy of the linearized high order PLL and the non linear PLL models (Figures 2 and 3 respectively) to describe the behavior of the real PLL, phase step tests were performed for both, and presented in Figures 9 (unit step) and 10 (40° step) respectively. Both phase settling times and overshoots are comparable to the experimental result (Test 1, Case 1).

## V. CONCLUSION

This paper shows that the exact modeling of the MA filter in discrete time domain, without using truncated Taylor series approximation [4], nor applying second order system modeling [8], neither approximating it by low order Padé equation [9], results in lower settling times compared to recent papers. Discrete root locus was employed to cope with the high order open loop transfer function. Tuning of the discrete PI compensator was done by pole placement of the dominant poles in a region defined by the specified ranges of settling time, natural frequency and damping factor. Experimental results confirm outstanding performance of the proposed method compared to current alternatives.

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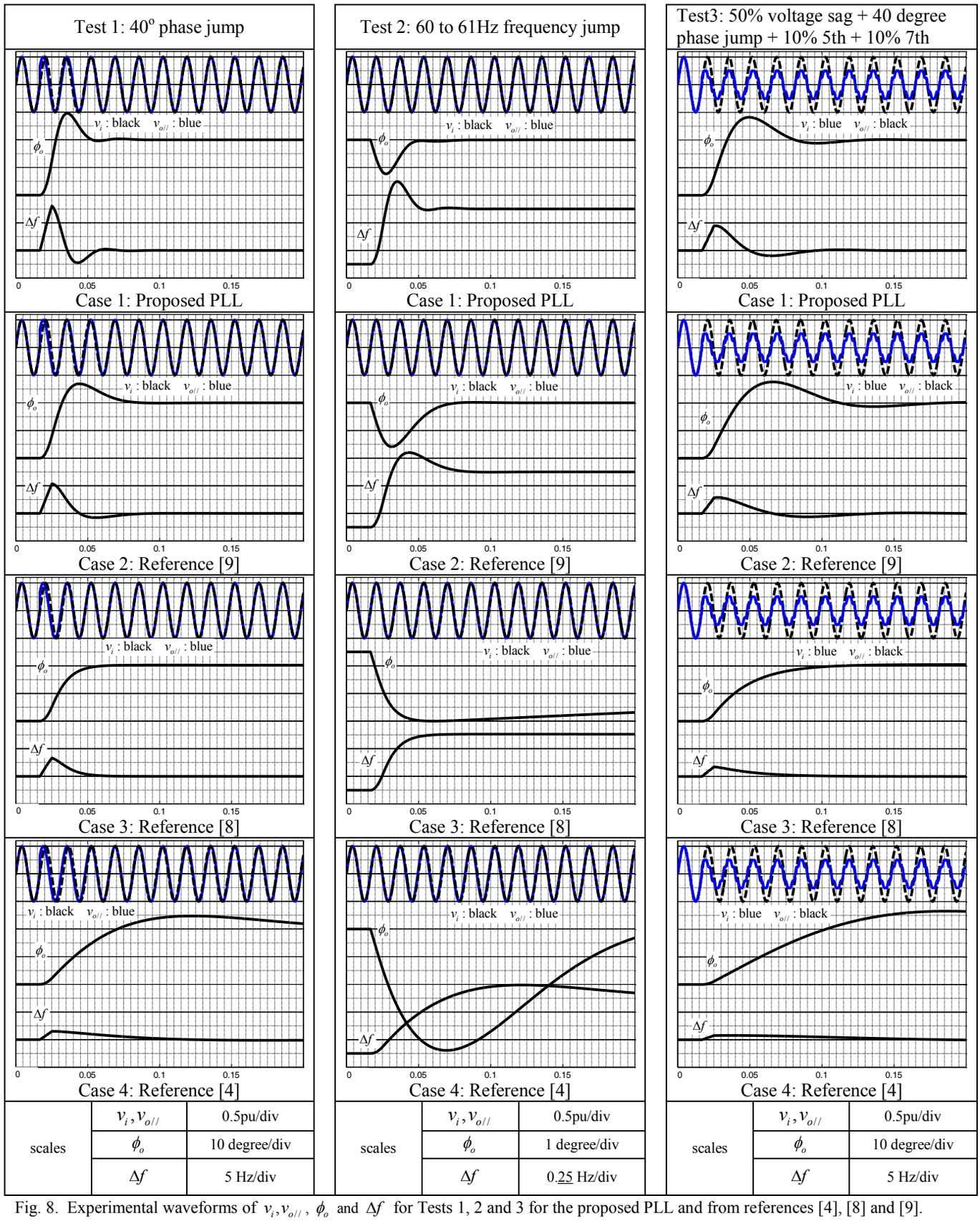


Fig. 8. Experimental waveforms of $v_i, v_{o//}$, $\phi_o$ and $\Delta f$ for Tests 1, 2 and 3 for the proposed PLL and from references [4], [8] and [9].

Test 1 - 0° to 40° phase jump at input $v_i$.

Test 2 - 60 Hz to 61 Hz frequency jump at input $v_i$.

Test 3 - 50% voltage sag + 40° phase jump + 10% 5th harmonic+ 10% 7th harmonic at input $v_i$.

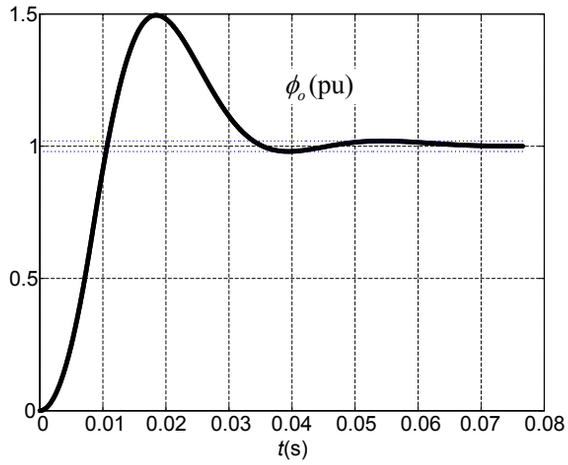


Fig. 9. Simulated unit-step response for the linearized model considering the proposed controller (2% settling time $t_s$ =2.035 cycles).

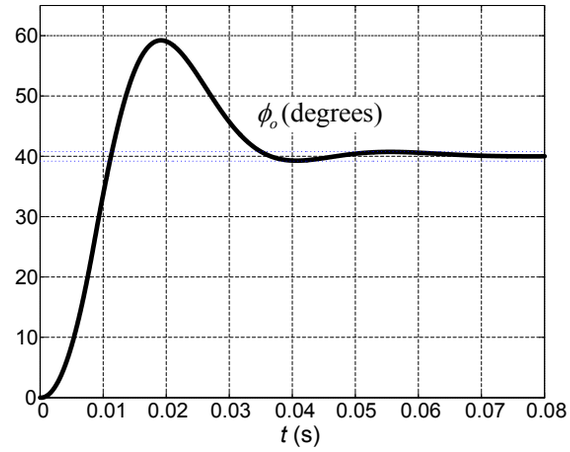


Fig. 10. Simulated 40° phase jump response for the complete PLL model considering the proposed controller (2% settling time $t_s$ =2.100 cycles).


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## BIOGRAPHIES

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